



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of : Gengying Gao)

Serial No.: 09/670,154)

Examiner: Trung Q. Nguyen

Filed: 9/26/2000)

Art Unit: 2829

For: METHOD OF TESTING THE)
ELECTROSTATIC DISCHARGE)
PERFORMANCE OF AN IC DEVICE)

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SUPPLEMENTAL APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Dear Sir:

The Appellants hereby submit this Supplemental Brief in triplicate in support of their request for reinstatement of the appeal after the examiner sought to reopen prosecution by way of Office action mailed August 13, 2003, after an Appeal Brief had been file. The Appellants respectfully request consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above patent application.

Serial No. 09/670,154

SUPPLEMENTAL APPEAL BRIEF

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I. REAL PARTY IN INTEREST

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II. RELATED APPEALS AND INTERFERENCES

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There are no related appeals or interferences

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III. STATUS OF THE CLAIMS

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Claims 1 to 20 are currently pending. No claims have been cancelled or added. Claims 1 to 20 stand rejected by the Examiner under the Final Rejection mailed December 18, 2002 and after the non-final rejection mailed 8/13/2003.

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Claims 1 to 20 stand rejected under 35 U.S.C. § 112, and under 35 U.S.C. § 102 as being unpatentable over Paniccia et al (US 5,872,360) and are being appealed.

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IV. STATUS OF AMENDMENTS

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Amendments to claims 1 and 8 were filed after the final rejection and were initially not entered on the premise that they would not place the application in a better form for appeal. However, the examiner subsequently reopened prosecution and thus the amendments stand as entered.

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V. SUMMARY OF INVENTION

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The invention deals with a new method of testing the resilience of an integrated circuit device to electrostatic discharge (ESD). In the past ESD resilience

involved a destructive approach involving discharging charge into the pins of the IC device. In contrast, the present invention provides a way of determining the ESD resilience in a non-destructive manner using a laser beam, and making a determination based on the amount of light reflected by the diffusion region of the IC compared to the amount of light absorbed by the diffusion region. This is described in the first paragraph of the Summary of the Invention (page 1, lines 22-24), page 3, lines 13-17, and page 4 lines 23-31 read with Figure 3.

Testing of ESD resilience has nothing to do with debugging a chip to determine whether it has defects. In fact, the chip may very well work fine but simply have a low ability to handle electrostatic discharges. It is a chip's ability to handle ESD that the present invention addresses, and it manages to do this in a non-destructive manner.

VI. ISSUES

The issues are whether the specification provides support for good ESD performance, and whether references dealing with the debugging of a chip or IC can be used in rejecting claims directed to a method of detecting resilience of a chip to ESD events.

Also, the question remains whether an explicit limitation in a claim dealing with a comparison of the light reflection results from a tested chip with light reflection results from a chip with known ESD resilience, can simply be ignored.

VII. GROUPING OF CLAIMS

Claims 1-20 were rejected based on the common argument that Paniccia et al anticipated each of the claims. Claim 1 is the only independent claim, with claims 2-20 depending from it.

104 **VIII. ARGUMENT**

105 Claim rejections - 35 USC 112

106 Claim 27 was rejected under 35 USC 112 as containing subject matter
107 which is not described in the specification.

108 It is respectfully pointed out that there is no claim 27 in the application.

109 Claim 1 was rejected on the basis that the specification and drawings do
110 not support good ESD performance, and that it is unclear what the characteristics
111 of good ESD performance were.

112 It is respectfully pointed out that ESD (Electrostatic Discharge) is a term
113 commonly used in the art of electronic devices and protection of electronic
114 devices. The high current associated with an ESD event can cause damage to
115 electronic circuit elements by exceeding the current handling capabilities of the
116 circuit elements. This is common knowledge in the art, hence ESD protection
117 devices are employed to shunt ESD current to ground, or alternatively the
118 devices are made self-protecting by making them more robust to be able to
119 withstand the high ESD currents. This invention deals with the latter situation
120 and provides a way of testing the resilience of the devices to ESD events. In fact,
121 the Discussion of the Prior Art section of the present application discusses the
122 issue of ESD resilience and the destructive nature of prior art ESD testing
123 techniques.

124 The examiner also argues that it is well known to all those skilled in the
125 art to use a laser beam to test the ESD.

126 The examiner, however, fails to disclose a single reference in support of this
127 contention except for citing Paniccia, which misstates what Paniccia stands for, as
128 is discussed in more detail below in response to the examiner's 35 USC 102
129 rejection.

130 The examiner also argues that the drawing and specification do not give
131 any support for I/O cells.

132 It is respectfully pointed out that page 4, lines 10-25 deal in detail with I/O cells
133 since I/O cells are the circuit elements typically exposed to ESD events.

134

135 Claim rejections - 35 USC 102

136 Claims 1-20 were rejected under 35 USC 102(b) over Paniccia.

137 It is respectfully submitted that Paniccia does not disclose testing ESD
138 performance. As discussed in response to the previous Office actions and in the
139 original Appeal Brief, (lines 103-110 on page 5), Paniccia does not deal with
140 testing of ESD resilience, and in fact nowhere states or suggests that it does so.
141 Paniccia, instead, discusses the problems of debugging a new product (col. 1,
142 lines 53-57). It then proposes a solution for determining voltage applied to a p-n
143 junction by monitoring the electric field by monitoring the electro-absorption of a
144 mode-locked laser (col. 7, lines 18-23).

145 Nowhere does Paniccia describe or suggest ways of monitoring ESD
146 performance of an IC device.

147 Claim 1, in contrast, specifically defines a method of monitoring ESD
148 performance. This is not a feature proposed in arguments or only in the
149 specification, but is specifically mentioned in claim 1.

150 However, in order to further distinguish the present invention from
151 Paniccia, claim 1 was amended to include the step of comparing the amount of
152 reflected light to the amount of reflected light from an I/O cell having good ESD
153 performance (see page 4, lines 23-31). This step also not present in Paniccia and is
154 not suggested anywhere in Paniccia.

155 Since the remaining claims 2-20 depend from claim 1, they will include the
156 new limitation, and are therefore also distinguishable over Paniccia.

157

158 As to claim 8, it is respectfully submitted that Paniccia does not mention
159 averaging a number of measurements. Nevertheless, claim 8 was amended to
160 specify that the samples are taken at the same I/O signal voltage level. This

161 further distinguishes from Paniccia, which clearly discusses measurements at
162 different electric fields and temperatures (Fig. 7 and col. 7, lines 7-17).

163
164 As to claim 15, it is respectfully submitted that Paniccia does not discuss
165 any testing in pre-packaged form. The section referred to by the examiner (col. 5,
166 lines 50-55) has to be read in the context of the rest of the sentence which clearly
167 states that it is often necessary to do the testing while the chip is packaged. In
168 other words the section specifically sets the context of the problem, namely
169 testing a packaged device. This is used by Paniccia to justify the need for a laser.
170 Nowhere does it mention or contemplate testing of unfinished devices.

171
172 As to claim 16, it is respectfully submitted that Paniccia does not disclose
173 that the device includes only some of its layers. The section referred to by the
174 examiner (col. 1, lines 62-67) merely states that a typical IC has multiple layers
175 and that it is therefore difficult to access nodes buried deep in the chip. There is
176 no mention of testing while there are only some of the layers formed.

177
178 Response to specific arguments raised by examiner

179
180 The examiner argued that ESD testing using a laser beam is known to all those
181 skilled in the art. This is entirely unsupported by any fact since there is no cited
182 reference to support this contention. Furthermore, claim 1 specifically includes
183 the limitation of comparing to an I/O cell having good ESD performance. This is
184 not disclosed or suggested in Paniccia or any other IC testing references.

185
186 The examiner argued that Paniccia discloses testing a device with only some of
187 its layers and that it disclosed using a continuous wave laser to probe the IC

188 device. As has been discussed above, Paniccia does not disclose a device having
189 only some of its layers (see arguments above).

190 It is unclear what the examiner's argument is regarding the use in Paniccia of a
191 continuous wave laser. In fact Paniccia specifically refers to using a mode-locked
192 laser. Fig 7 and col. 8, lines 6-15 of Paniccia specify a mode-locked laser, not a
193 continuous wave laser. In any event the present application uses the continuous
194 wave laser simply as one way of positioning the mode-locked laser. Paniccia
195 does not disclose using a continuous wave laser as a positioning means or for
196 any other purpose for that matter.

197 In any event, all of the dependent claims depend from claim 1 and therefore
198 include the limitations of claim 1, and are therefore, by that reason alone,
199 distinguishable over the prior art.

200
201 The examiner states that any special structural or functional aspects of the
202 Applicant's invention have to be clear from the claims themselves, and goes on to
203 state various case law. The examiner's arguments, while correct, do not bear on
204 the present facts where the limitations are specifically recited in the claims. The
205 claims themselves include the limitation of testing ESD performance and also
206 include the limitation of comparing reflected light to the light reflected from an
207 I/O cell with good ESD performance. Each of these limitations explicitly
208 distinguish over the cited art.

209
210 In view of the fact that claim 1 specifically deals with testing of ESD performance
211 and is further amended to specifically include the limitation of comparing the
212 light reflected to the light reflected from an I/O cell with good ESD performance,
213 it is respectfully submitted that all of the claims are distinguishable over the prior
214 art. Furthermore, claims 10, 15, 16, 18 add additional limitations not disclosed in

215 Paniccia.

216 Allowance of all of the claims is therefore respectfully requested.

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Charge Our Deposit Account

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If there are any further charges not accounted for herein, please charge

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them to our deposit account No. 140448

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Respectfully submitted,

Vollrath & Associates

Date: 11/11/ 2003



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IX. APPENDIX

1. A method of testing the ESD performance of an IC device, comprising
probing the device with a laser beam,
monitoring the amount of light reflected from the device, and
comparing the amount of light reflected to the amount of light
reflected from an I/O cell having good ESD performance.
2. A method of Claim 1, wherein the laser beam is used to probe the IC
device.
3. A method of Claim 2, wherein the energy of the laser beam
corresponds substantially to the bandgap of the substrate of the
device.
4. A method of Claim 3, wherein the substrate is silicon and the energy of
the laser beam is about 1.1eV.
5. A method of claim 3, wherein the diffusions of the IC device are
probed with the laser beam.
6. A method of Claim 5, wherein in the device is probed through the back
of the device.
7. A method of Claim 6, wherein the diffusions of I/O cells are probed to
determine how much light is absorbed and how much light is reflected
by the diffusions.
8. A method of Claim 5, wherein several samples are taken of each
probed location, at the same I/O signal voltage level, and the results
averaged.
9. A method of Claim 1, wherein a mode-locked laser is used to probe
the IC device.
10. A method of Claim 9, wherein a continuous wave laser is used in
addition to the mode-locked laser, to provide an image of the IC device
in order to facilitate the positioning of the beam of the mode-locked
laser.
11. A method of Claim 9, wherein the mode-locked laser is positioned by a
user.

- 291 12. A method of Claim 9, wherein the mode-locked laser is positioned
292 automatically using image recognition.
- 293 13. A method of Claim 5, wherein power is supplied to the device during
294 testing.
- 295 14. A method of Claim 13, wherein the testing is performed on the device
296 in a packaged form.
- 297 15. A method of Claim 13, wherein the testing is performed on the device
298 in a prepackaged form.
- 299 16. A method of Claim 15, wherein the device includes only some of its
300 layers.
- 301 17. A method of Claim 6, wherein a mode-locked laser is used to probe
302 the IC device.
- 303 18. A method of Claim 17, wherein a continuous wave laser is used in
304 addition to the mode-locked laser, to provide an image of the IC device
305 in order to facilitate the positioning of the beam of the mode-locked
306 laser.
- 307 19. A method of Claim 17, wherein the mode-locked laser is positioned by
308 a user.
- 309 20. A method of Claim 17, wherein the mode-locked laser is positioned
310 automatically using image recognition.
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